# Sheet 7

**4.1** The input status bit in an interface circuit is cleared as soon as the input data buffer is read. Why is this important?

**4.3** The address bus of a computer has 16 address lines, $A_{15-0}$. If the address assigned to one device is $7CA4_{16}$ and the address decoder for that device ignores lines $A_8$ and $A_9$, what are all the addresses to which this device will respond?

**4.4** What is the difference between a subroutine and an interrupt-service routine?

**4.5** The discussion in this chapter assumed that interrupts are not acknowledged until the current machine instruction completes execution. Consider the possibility of suspending operation of the processor in the middle of executing an instruction in order to acknowledge an interrupt. Discuss the difficulties that may arise.

**4.6** Three devices, A, B, and C, are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases:

(*a*) The computer has one interrupt-request line.

(*b*) Two interrupt-request lines, INTR1 and INTR2, are available, with INTR1 having higher priority.

Specify when and how interrupts are enabled and disabled in each case.

**4.12** A logic circuit is needed to implement the priority network shown in Figure 4.8*b*. The network handles three interrupt request lines. When a request is received on line INTR*i*, the network generates an acknowledgment on line INTA*i*. If more than one request is received, only the highest-priority request is acknowledged, where the ordering of priorities is

priority of INTR1 > priority of INTR2 > priority of INTR3

(*a*) Give a truth table for each of the outputs INTA1, INTA2, and INTA3.

(*b*) Give a logic circuit for implementing this priority network.

(*c*) Can your design be easily extended for more interrupt-request lines?

(*d*) By adding inputs DECIDE and RESET, modify your design such that INTA*i* is set to 1 when a pulse is received on the input DECIDE and is reset to 0 when a pulse is received on the input RESET.

**4.13** Interrupts and bus arbitration require means for selecting one of several requests based on their priority. Design a circuit that implements a rotating-priority scheme for four input lines, REQ1 through REQ4. Initially, REQ1 has the highest and REQ4 the lowest priority. After some line receives service, it becomes the lowest priority line, and the next line receives highest priority. For example, after REQ2 has been serviced, the priority order, starting with the highest, becomes REQ3, REQ4, REQ1, REQ2. Your circuit should generate four output grant signals, GR1 through GR4, one for each input request line. One of these outputs should be asserted when a pulse is received on a line called DECIDE.

**4.19** The interrupt-request line, which uses the open-collector scheme, carries a signal that is the logical OR of the requests from all the devices connected to it. In a different application, it is required to generate a signal that indicates that all devices connected to the bus are ready. Explain how you can use the open-collector scheme for this purpose.

**4.20** In some computers, the processor responds only to the leading edge of the interrupt-request signal on one of its interrupt-request lines. What happens if two independent devices are connected to this line?

**4.28** An industrial plant uses several limit sensors for monitoring temperature, pressure, and other factors. The output of each sensor consists of an ON/OFF switch, and eight such sensors need to be connected to the bus of a small computer. Design an appropriate interface so that the state of all eight switches can be read simultaneously as a single byte at address $FE10_{16}$. Assume the bus is synchronous and that it uses the timing sequence of Figure 4.24.